MAGNETIC MEMORY ELEMENT HAVING CONTROLLED NUCLEATION SITE IN DATA LAYER

BACKGROUND

[0001] Consider the example of a Magnetic Random Access Memory (MRAM) device. The device includes a resistive cross point array of magnetic tunnel junctions. Each magnetic tunnel junction is located at a cross point of a word line and a bit line, and has a magnetization that assumes one of two stable orientations at any given time. These two stable orientations, parallel and anti-parallel, represent logic values of '0' and '1.

[0002] A write operation on a "selected" magnetic tunnel junction may be performed by supplying write currents to the word and bit lines crossing the selected magnetic tunnel junction. The write currents create two orthogonal external magnetic fields. The magnetic tunnel junctions are designed to switch (from parallel to anti-parallel or vice versa) only in the presence of the two orthogonal magnetic fields.

[0003] A "half-selected" magnetic tunnel junction lies along only one line that is supplied with a write current (either a bit line or a word line). Thus, a half-selected magnetic tunnel junction is exposed to only one external magnetic field during a write operation. The magnetic tunnel junctions are designed not to switch in the presence of a single magnetic field.

[0004] In practice, however, switching distributions of the magnetic tunnel junctions in an MRAM array are large, and the switching fields of nominally similar magnetic tunnel junctions are non-uniform. Some half-selected magnetic tunnel junctions switch in the presence of only a single external magnetic field, and some selected magnetic tunnel junctions do not switch in the presence of two orthogonal magnetic fields.

[0005] A write error occurs if the magnetization orientation of a selected magnetic tunnel junction is not switched, or if the magnetization orientation of a half-selected magnetic tunnel junction is inadvertently switched. In a large MRAM array, many write errors can place a substantial burden on error code correction.

SUMMARY

[0006] According to one aspect of the present invention, a ferromagnetic data layer of a magnetic memory element is formed with a controlled nucleation site. Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 is an illustration of an MRAM device according to an embodiment of the present invention.

[0008] Figure 2 is an illustration of a magnetic memory element of the MRAM device.

[0009] Figure 3 is an illustration of a hysteresis curve for the magnetic memory element.

[0010] Figure 4 is an illustration of an array of data layers in the MRAM device.

[0011] Figures 5a-5f are illustrations of data layers having different types and arrangements of controlled nucleation sites.

[0012] Figure 6 is an illustration of a method of fabricating an MRAM device according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0013] As shown in the drawings for purposes of illustration, the present invention is embodied in an MRAM device including an array of magnetic memory elements. Data layers of the MRAM device have controlled nucleation sites. The controlled nucleation sites improve switching distribution of the magnetic memory elements, which increases reliability of writing to the magnetic memory elements.

[0014] Reference is now made to Figure 1, which illustrates an MRAM device 10 including an array 12 of memory cells 14. The memory cells

14 are arranged in rows and columns, with the rows extending in an x-direction and the columns extending in a y-direction. Only a relatively small number of memory cells 14 are shown to simplify th description of the device 10. In practice, arrays of any size may be used.

[0015] Word lines 16 extend in the x-direction of the memory cell array 12, and bit lines 18 extend in the y-direction of the memory cell array 12. There may be one word line 16 for each row of the array 12 and one bit line 18 for each column of the array 12. Each memory cell 14 is located at a cross point of a word line 16 and bit line 18.

[0016] The MRAM device 10 also includes a read/write circuit (not shown) for performing read and write operations on the memory cells 14. The read/write circuit senses the resistance states of selected memory cells during read operations. The read/write circuit supplies write currents to selected word and bit lines 16 and 18 during write operations.

[0017] Each memory cell 14 includes at least one magnetic memory element. The magnetic memory elements may be magnetic tunnel junctions, giant magneto-resistive (GMR) devices, AMR devices, or any other magnetic memory device in which a data layer is switched. These devices include ferromagnetic data and reference layers separated by a spacer layer. If the magnetic memory element is a GMR device, the spacer layer is made of a conductive material such as copper. If the magnetic memory element is a magnetic tunnel junction, the spacer layer is an insulating tunnel barrier made of a material such as Al_2O_3.

[0018] Additional reference is made to Figure 2, which shows an exemplary magnetic memory element 50. The exemplary magnetic memory element 50 is a magnetic tunnel junction including a pinned layer 52, a data layer 54, and an insulating tunnel barrier 56 between the pinned and data layers 52 and 54. The pinned layer 52 has a magnetization (represented by vector M1) that is oriented in the plane of the pinned layer 52 but fixed so as not to rotate in the presence of an applied magnetic field in a range of interest. The data layer 54 has a magnetization (represented by vector M2) that is not pinned. Rather, the magnetization can be oriented in either of two directions

along an axis (the "easy" axis) lying in the plane of the data layer 54 (one direction is shown in solid, and the other direction is shown in dashed). If the magnetization vectors (M1 and M2) of the pinned and data layers 52 and 54 point in the same direction, the orientation of the magnetic tunnel junction is said to be "parallel". If the magnetization of the pinned and data layers 52 and 54 layers point in opposite directions, the orientation of the magnetic tunnel junction is said to be "anti-parallel."

[0019] The insulating tunnel barrier 56 allows quantum mechanical tunneling to occur between the data and pinned layers 54 and 52. This tunneling phenomenon is electron spin dependent, making the resistance of the magnetic tunnel junction a function of the relative orientations of the magnetization of the pinned and data layers 52 and 54. The magnetization orientation and, therefore, the stored logic value may be read by sensing the resistance state of the magnetic tunnel junction.

[0020] The write currents create magnetic fields about the word and bit lines 16 and 18 crossing the selected memory cell. When combined, these two magnetic fields exceed the coercivity of the data layer and cause the magnetization vector (M1) of the data layer 54 to assume a desired orientation. A hysteresis curve for the magnetic tunnel junction is shown in Figure 3. Coercivity is denoted by Hc. When the combined magnetic field exceeds the coercivity, the magnetic tunnel junction can be switched.

[0021] Reference is now made to Figure 4, which shows a plurality of data layers 54 in the array 12 of the MRAM device 10. The data layers 54 have controlled nucleation sites 58. The nucleation sites 58 are regions where the reversal of magnetization is initiated. They have a lower switching threshold relative to the neighboring regions 60 of the data layer 54. The nucleation sites 58 are controlled in that they have the same locations in the data layers 54 of all memory cells in the array 12. The locations are preferably along edges of the data layers 54, and more preferably near corners.

[0022] Nucleation, the initiation of switching reversal, occurs at the nucleation sites 58. Since a nucleation site 58 is not fully surrounded by the neighboring region 60 of the data layer 54, magnetic exchange interaction

between the nucleation site 58 and the neighboring region 60 of the data layer 54 is reduced, and only occurs at the boundary of the neighboring region 60 and the nucleation site 58. As a result, switching reversal always begins at the nucleation site 58, even if the neighboring region 60 contains defects.

[0023] If the nucleation sites 58 are formed along the edges on the data layers 54, the randomness of nucleation is reduced. Consequently, switching distribution (the distribution of coercivities) of the memory cells 14 in the device 10 is more uniform.

[0024] The nucleation sites 58 may be protrusions from the data layers 54 or divets in the data layers 54. The shape of the divets or protrusions may be circular, elliptical, rectangular, or any other shape.

[0025] Size of the nucleation sites 58 may be between 0.25W and 0.75W, where W is the width of the data layer 54. However, the size of the nucleation sites 58 is not limited to that range. The size of the nucleation sites 58 may be much smaller than W, for example, in the range of 0.05W to 0.1W.

[0026] The nucleation sites 58 may be as thick as, or thicker than, the data layer 54. Thus the protrusions may be as thick as the data layer 54, and the divets may extend through the data layer 54.

[0027] The size and shape of the nucleation sites 58 across the array 12 may be uniform. Uniform size and shape across the array 12 should improve uniformity of nucleation energy.

[0028] The data layers 54 are not limited to the nucleation sites 58 shown in Figure 4. Other type and arrangements of nucleation sites are shown in Figures 5a-5f. Figures 5a, 5b, 5c 5f show that the nucleation sites 58 may be protrusions instead of divets, Figures 5b-5f shows that a data layer 54 may have more than one nucleation site 58; and Figures 5b, 5e and 5f show that two nucleation sites 58 may be formed at different edges.

[0029] In Figures 5b-5e the nucleation sites 58 are shown as having a symmetric arrangement on the data layers 54. However, they are not so limited. For example, Figure 5f shows the nucleation sites 58 have a non-symmetric arrangement. The non-symmetric arrangement may be used to compensate for an offset in switching fields. For example, one site might

nucleate at a higher switching field for one direction, and a lower switching for the other direction. Thus the offset is balanced out due to magnetostatics.

[0030] Reference is now made to Figures 6, which illustrates the fabrication of a first level of an MRAM device. The fabrication will be described in connection with magnetic tunnel junctions.

[0031] The read/write circuit and other circuits are formed in a silicon substrate (110). Bit lines are formed on the substrate (112). A stack of magnetic memory element material is deposited (114). A stack for magnetic tunnel junctions may include pinned ferromagnetic layer material, insulating tunnel barrier material, and data layer material. The data layer material may be deposited before or after the pinned layer material.

[0032] Bits are formed (116). Lithography (e.g., photolithography, e-beam lithography) may be used to define a pattern on the stack, and bits may be formed by a process such as ion milling, chemical etching, drying etching, etc. The patterns include the definitions of the nucleation sites. Thus the nucleation sites (e.g., protrusions, divets) are formed during formation of the bits.

[0033] A hard mask may be used during bit formation to define the bits (including the nucleation sites). An advantage of the hard mask is that it reduces edge roughness and allows the bits to be formed closer together.

[0034] Each bit may be milled down to its pinned layer. As a result, a nucleation site may also be formed on each pinned layer, as well as each data layer.

[0035] Gaps between the bits are filled in with an isolation dielectric (118). Then bit lines are deposited (120).

[0036] Additional levels may be added to the MRAM device. An insulation material such as silicon dioxide is deposited on the last level, and a new level is fabricated by repeating steps 112-120.

[0037] The MRAM device may be used in a variety of applications. For example, the MRAM device may be used for long term data storage in devices such as solid state hard drives and digital cameras. It may be used for embedded applications such as extremely fast processors and network

appliances.

[0038] The present invention is not limited to the specific embodiments described and illustrated above. Instead, the invention is construed according to the claims that follow.